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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/752,131	01/06/2004	Hae-Seung Lee	7033C	3915

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EXAMINER	
HSU, AMY R	

ART UNIT	PAPER NUMBER
2622	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/752,131	LEE ET AL.	
	Examiner	Art Unit	
	Amy Hsu	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 July 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments, filed 7/30/12007, with respect to the rejection(s) of claim(s) 1-21 under 35 USC §103 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. The rejections of Claims 1-21 have been withdrawn and moot in view of the new groups of rejection. This Office Action is Non-Final and meant to replace the Non-Final Office Action (mailed May 11, 2007).

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kuroda et al. (US 6512543) in view of Weale et al. (US 7286174).

Regarding Claim 1, Kuroda teaches a circuit for a pixel site in an imaging array (*Fig. 1 shows a circuit for a pixel, reference number 32, in an imaging array)*, comprising: a pixel to convert incident light to an electrical signal (*Fig. 1, the pixel 32 includes a photodiode, reference number 33)*; a row line to read out a voltage from said pixel (*reference number 49 is a row line)*; a row line transistor (*reference number 59 is a row reset transistor which resets the charges in the photoelectric sections in a row as taught in Col 7 Lines 6-17)*, operatively connected between one end of said row line and

taught in Col 7 Lines 6-17), operatively connected between one end of said row line and a predetermined voltage (*reference number 59 is connected between 49, the row line, and 58, a voltage supply which supplies a predetermined voltage according to the reset method to be described below)*, to reset a voltage associated with said row line (*Col 7 Lines12-16)*; and a reset voltage generator, operatively connected to said row line transistor, to generate reset pulses (*reference number 58, reset voltage input portion which supplies voltage, Col 8 Lines 28-32)*. Kuroda teaches this circuitry and further teaches reset by row, however Kuroda dose not focus on optimizing the reset function and does not further teach a method of reset. Since Kuroda simply teaches the pixel is reset, one of ordinary skill in the art would be left with the choice of hard reset, soft reset, or combinations thereof. In order to optimize the reset function using this row connected circuitry, one of ordinary skill would look to prior art to determine which method of reset would produce best results.

Weale teaches a way to optimize the reset method in order to reduce noise and image lag while producing the best quality. Col 12 Lines 13-25 teaches that the pixel is reset before integration, then integration is performed, then the photo site is reset again. Weale teaches this reset method in more detail and it is a known method to eliminate image lag and fat zero noise.

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the teaching of Kuroda to enhance quality by reducing image noise and image lag by resetting by the method taught above. Weale teaches the preferred reset method, but it can be applied to the circuitry taught by Kuroda which generates a

reset pulse to an entire row. It would be obvious to modify Kuroda by generating a reset pulse to an entire row before integration and after integration to both obtain the benefits of being able to control all pixels in a row simultaneously and also to reduce image lag by resetting after integration which leave the photo detector at a potential equal to the first voltage minus threshold voltage regardless of charge remaining from a previous integration, thus eliminating image lag.

Regarding Claim 2, Kuroda teaches the circuit as claimed in claim 1, wherein said pixel comprising: a light-detecting element to convert incident light to a photocurrent *(Fig. 1 reference number 33)*; a reset transistor (*reference number 60)*, operatively connected to said light-detecting element, to reset a voltage associated with said light-detecting element (*Col 7 Lines 12-16)*; and a pixel reset voltage generator, operatively connected to a non-gate terminal of said reset transistor, to generate a reset voltage (*Fig. 1 and Col 7 Lines 6-18).* The paragraph regarding Claim 1 addresses the limitation of generating a first pixel reset voltage and a second reset voltage after generating first voltage.

Regarding Claim 3, Kuroda in view of Weale teach the circuit as claimed in claim 1, and Weale further teaches the first reset before the start of integration is done in order to provide a known starting point (*Col 12 Lines 6-8).* It would have been obvious to one of ordinary skill in the art at the time of the invention to set the known starting

point to ground so a voltage does not have to be generated as a known starting point, thus saving power.

Regarding Claim 4, Kuroda teaches the circuit as claimed in claim 2, wherein said pixel further comprising: a transistor (*Fig. 1 reference number 34)*; said transistor having a gate thereof operatively connected to said light-detecting element (*see Fig. 1*); said transistor having a non-gate terminal thereof operatively connected to said pixel reset voltage generator (*non-gate of reference number 34 is connected to 58, which provides voltage pulses to reset the row).*

Regarding Claim 5, Kuroda teaches the circuit as claimed in claim 2, wherein said pixel further comprising: a transistor; said transistor having a gate thereof operatively connected to said light-detecting element (*as addressed with Claim 4)*; said transistor having a non-gate terminal thereof operatively connected to a voltage source (*the non-gate terminal closer to the top of the drawing is connected to Vdd).*

Regarding Claim 6, Kuroda in view of Weale teach the circuit as claimed in claim 2, and Weale further teaches the first pixel reset voltage has a value to drive said reset transistor to operate in a triode region (*Col 12 Lines 40-45 teaches the first voltage level is desired for the photo detector at a beginning of the integration cycle in order to hard reset the photo site).* Paragraph 40 of the instant application defines the triode

region as a triode region of operation for hard reset. It would have been obvious to combine the teaching of Weale with that of Kuroda for the same rationale as with claim

Regarding Claim 7, Kuroda teaches pixel circuitry using a row line, which resets all pixels in a row since they are connected in that way as seen in Fig. 1. Kuroda teaches a reset pulse, (*Fig. 2 reference number 71)* and simply teaches a single pulse and does not focus on optimizing reset method. Therefore one of ordinary skill in the art would look to prior art to determine the best combination of resetting of the pixel to optimize quality.

Weale teaches a method for measuring a pixel voltage comprising: (a) hard resetting the row line voltage to a first predetermined voltage; (b) soft resetting the row line voltage to a first pixel voltage; (c) hard resetting the row line voltage to a second predetermined voltage; (d) soft resetting the row line voltage to a second pixel voltage (*Col 12 Lines 13-25)*; and (e) determining a difference between the first and second pixel voltages, the difference being the measured pixel voltage (*Col 13 Lines 22-27 teaches that a signal level is sampled then the pixel is reset for a second time and sampled again and the difference between these two samples, having been reset in between, is the output signal).*

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teaching of Kuroda with that of Weale to realize an imaging array that can be reset by rows, and the method of reset is such a method to reduce

image lag and image noise by hard resetting before soft resetting and measuring the voltage twice to obtain a difference as the output signal to optimize quality.

Regarding Claim 8, Kuroda in view of Weal teaches the method as claimed in claim 7, and Weale further teaches hard reset is performed to provide a known starting point. It would have been obvious to one of ordinary skill in the art at the time of the invention to set the known starting point to the same level both times to ensure consistency of the known starting point.

Claim 9-11 is rejected similarly to Claim 3.

Regarding Claim 12, Kuroda in view of Weale teach the method as claimed in claim 7, and Weale further teaches the first pixel voltage is a pixel reset voltage and the second pixel voltage is a pixel integrated voltage (*Col 12 Lines 13-25 teaches that the first set of resets occurs to reset the photo site before integration and is therefore the reset voltage, and the second set of resets occurs after integration and is therefore the integrated voltage).* It would have been obvious to combine the teachings of Weale for the reasons set forth with Claim 7.

Regarding Claim 13, Kuroda in view of Weale teach the method as claimed in claim 7, but does not specifically teach the second pixel voltage is a pixel reset voltage and the first pixel voltage is a pixel integrated voltage. However, Weale teaches a

reset voltage and then an integration voltage (*Col 12)* and it would have been obvious to one of ordinary skill in the art at the time of the invention to measure the integration voltage and the next period's reset voltage to also obtain the difference between the two as an output signal because this order is dependent on how the circuit most optimally reads out the signals and would produce the same effective result as reading the reset first and the integrated voltage second.

Regarding Claim 14, Kuroda in view of Weale teach the method as claimed in claim 7, Weale further teaches (f) generating a hard reset of a voltage associated with a light-detecting element of the pixel to reset the voltage associated with the light-detecting element; and (g) generating a soft reset of the voltage associated with the light-detecting element, after generating the hard reset, to reset the voltage associated with the light-detecting element (*Col 12 Lines 13-25 teaches generating a hard then soft reset to reset the photodiode).* It would have been obvious to combine for the same rationale as with Claim 7.

Regarding Claim 15, Kuroda teaches a pixel circuit in an imaging array with pixels of a row connected by a row line, (*Fig. 1 reference number 49)* and pixels of a column connected by a column line (*reference number 43).* Kuroda teaches simply a reset pulse by the reset voltage generator which sends a reset pulse to the row line through the row line transistor, 59. One of ordinary skill in the art would be left with the

choice of hard, soft reset and combinations to most optimize the procedure one would look to prior art for known methods to apply to the circuitry of Kuroda.

Weale teaches a method for measuring a pixel voltage by resetting a first predetermined voltage level, then another reset to a pixel voltage level, and capturing a voltage, then to repeat the procedure and determine the difference as the output voltage (*Col 12 Lines 12-25 and Col 13 Lines22-26).*

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the teaching of Kuroda by applying the concept of resetting taught by Weale in order to optimize quality by reducing image lag and image noise by the method of Weale. To apply Weale to Kuroda, setting the first predetermined voltage would require turning on the row line transistor because this transistor sets the reset voltage for all the pixels in the corresponding row. In order to apply the next part taught by Weale to get the voltage level to the pixel voltage level, in a row connected circuitry, the row line transistor would turn off after the first predetermined voltage is set and the column select transistors (*for example Kuroda Fig. 1 reference number 53)* would turn on to bring the row line voltage to the pixel voltage level. To apply Weale to Kuroda, this would occur twice with the voltage measured after each set of reset and the difference taken to realize the output voltage. It would be obvious to apply Weale to Kuroda because the reset method of Weale uses the first and second predetermined voltage resets to eliminate lag and pixel to pixel variations in the reset level, while the soft resets fully depletes the photodiode of charge to eliminate kTC noise generated by the hard reset. This reset method taught by Weale would have been realize to one of

ordinary skill in the art to optimize the benefits of both hard and soft reset to provide the best quality in the image sensor.

Claims 16-21 are rejected similarly to Claims 8-13.

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Nakamura et al. (US 2004/0201550) teaches an image sensor with photoreceptors arranged in a pixel array with column lines and read out circuitry on the column lines.

Mendis et al. (US 6958776) teaches an apparatus for reducing image lag in CMOS active pixel sensors at low light levels by controlling the reset level.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Amy Hsu whose telephone number is 571-270-3012. The examiner can normally be reached on M-F 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lin Ye can be reached on 571-272-7372. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Amy Hsu
Examiner
Art Unit 2622

ARH 11/11/07

LIN YE
SUPERVISORY PATENT EXAMINER